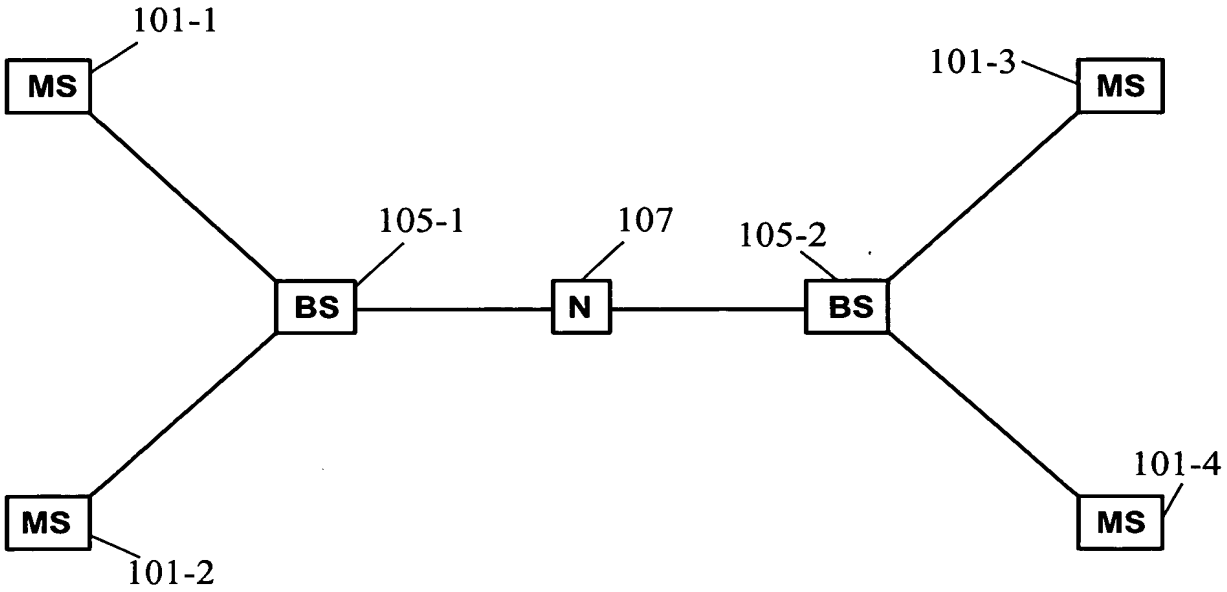

FIG. 1

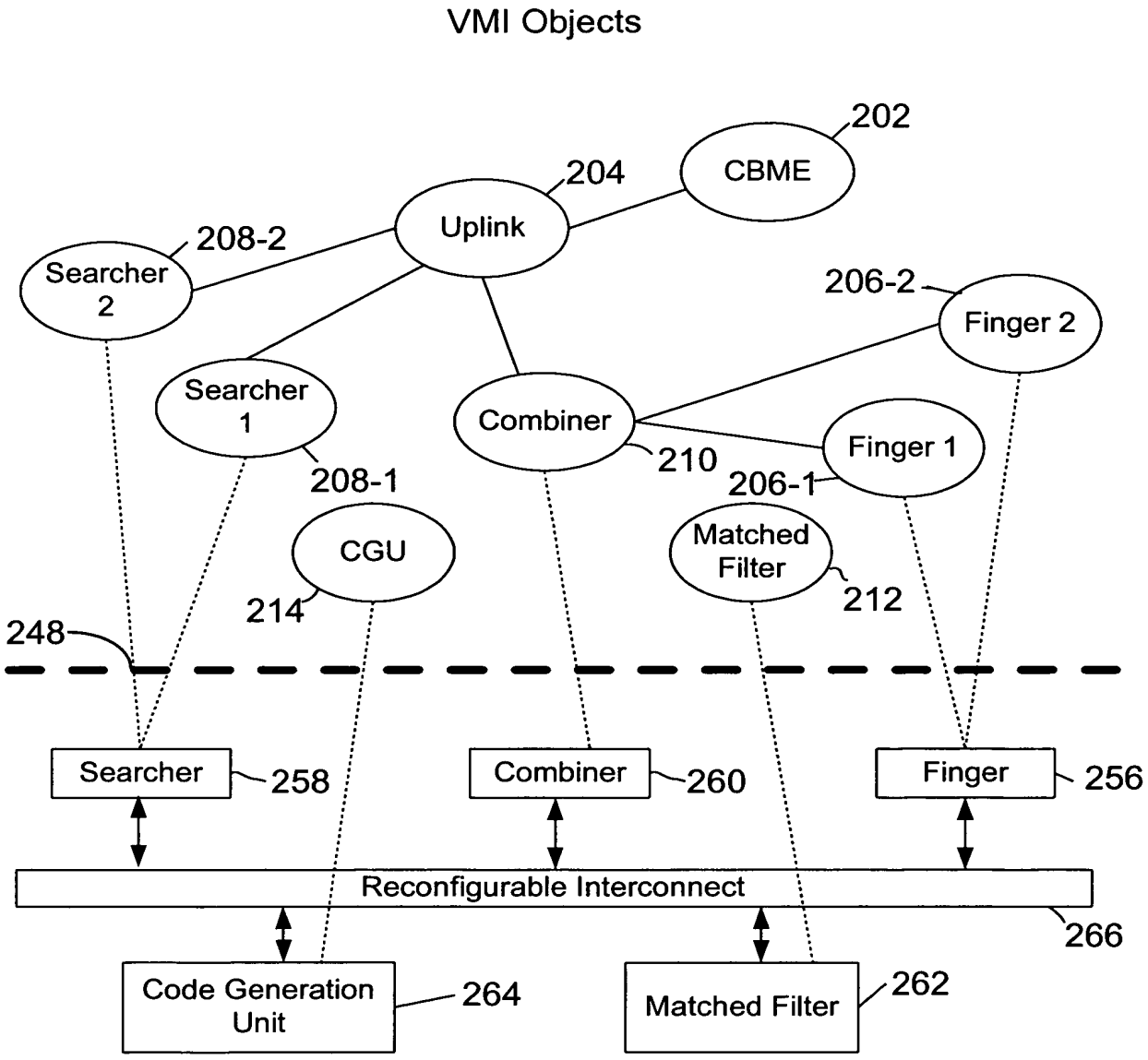
VMI Objects
202
CBME
204
Uplink
208-2
Searcher 2
206-2
Finger 2
Searcher 1
Combiner
210
Finger 1
208-1
206-1
CGU
214
Matched Filter
212
248
Searcher
258
Combiner
260
Finger
256
Reconfigurable Interconnect
266
Code Generation Unit
264
Matched Filter
262
Hardware Kernels

FIG. 2

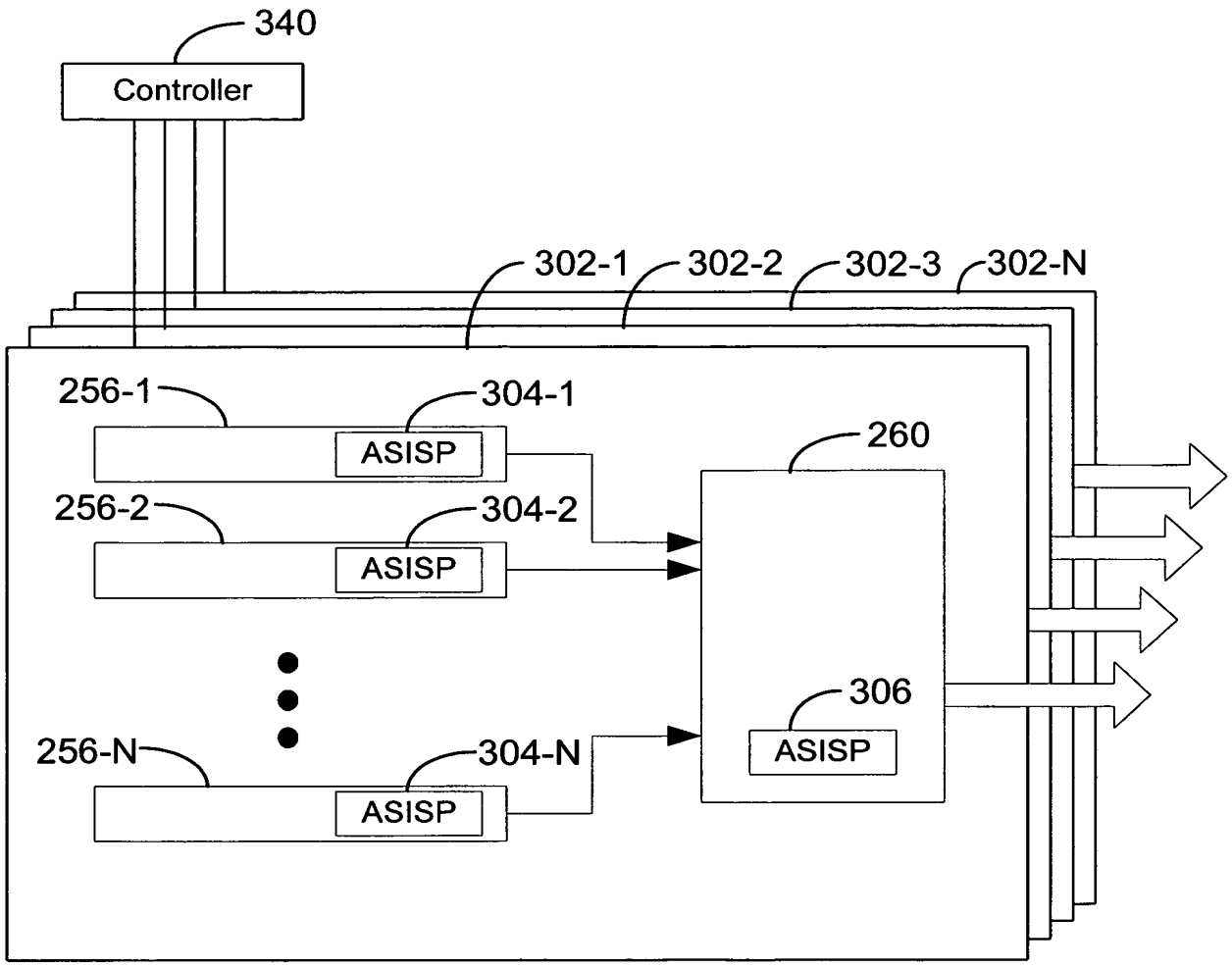
340
Controller
302-1
302-2
302-3
302-N
256-1
304-1
ASISP
260
256-2
304-2
ASISP
306
ASISP
256-N
304-N
ASISP

FIG. 3

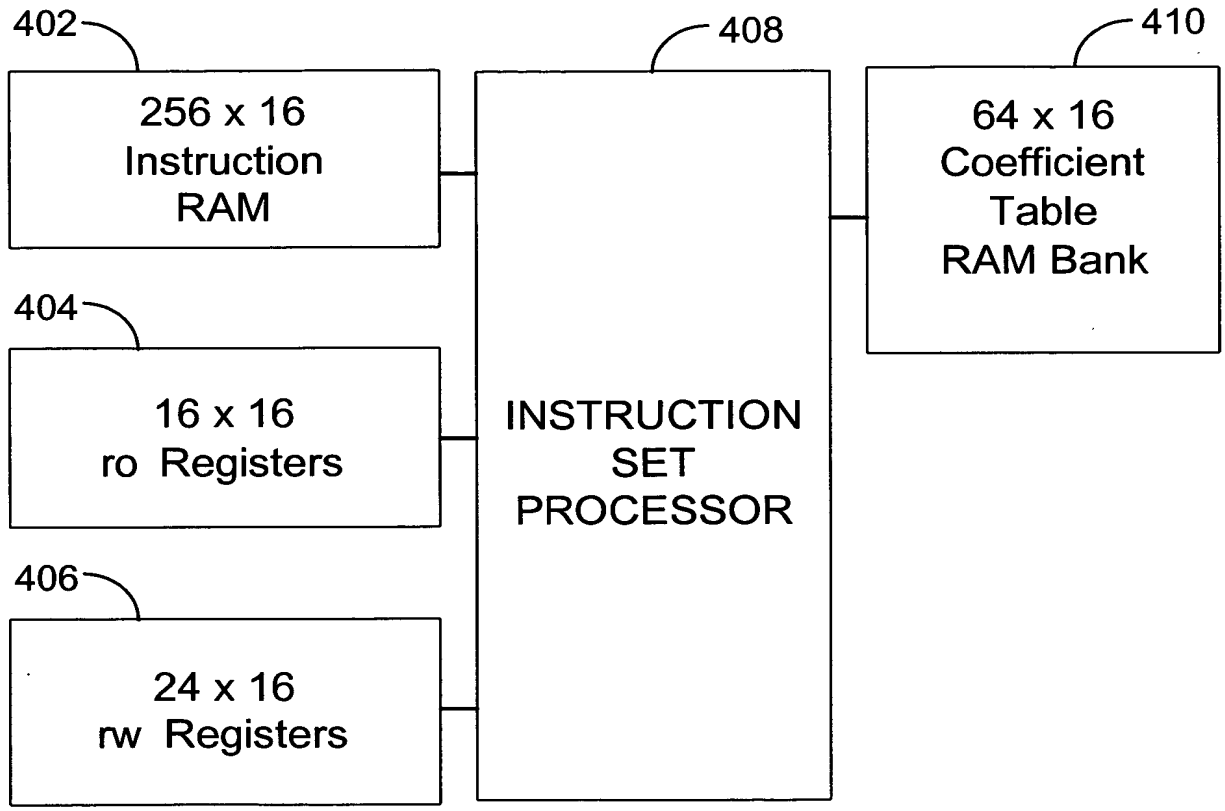
402
256 x 16
Instruction
RAM
404
16 x 16
ro Registers
406
24 x 16
rw Registers
408
INSTRUCTION
SET
PROCESSOR
410
64 x 16
Coefficient
Table
RAM Bank

FIG. 4

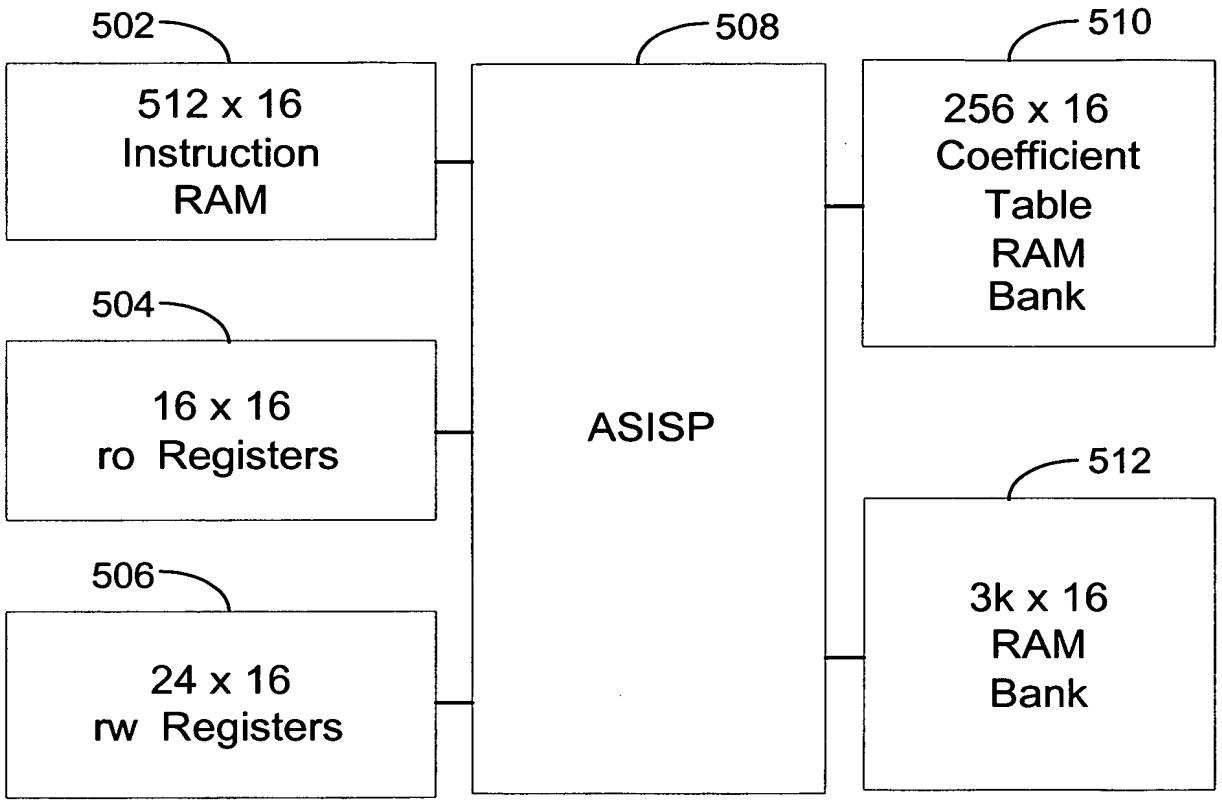
502
512 x 16
Instruction
RAM
504
16 x 16
ro Registers
506
24 x 16
rw Registers
508
ASISP
510
256 x 16
Coefficient
Table
RAM
Bank
512
3k x 16
RAM
Bank

FIG. 5

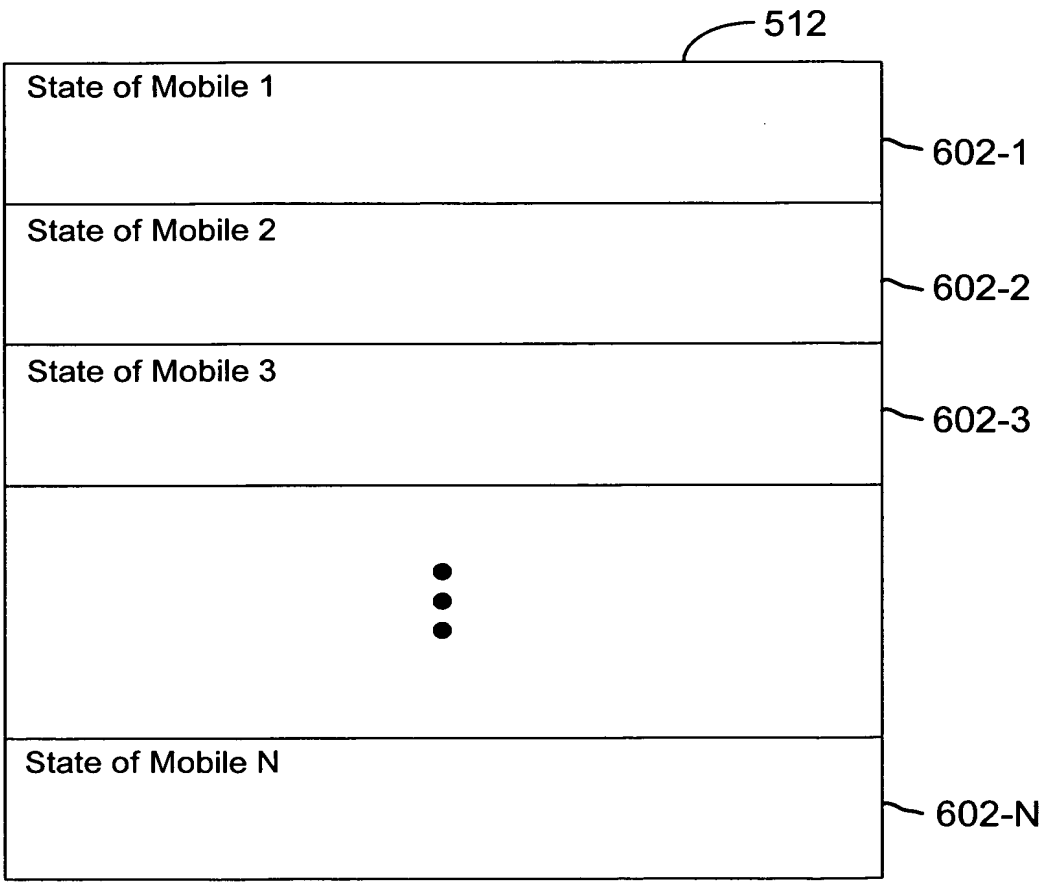
512
State of Mobile 1
602-1
State of Mobile 2
602-2
State of Mobile 3
602-3
State of Mobile N
602-N

FIG. 6

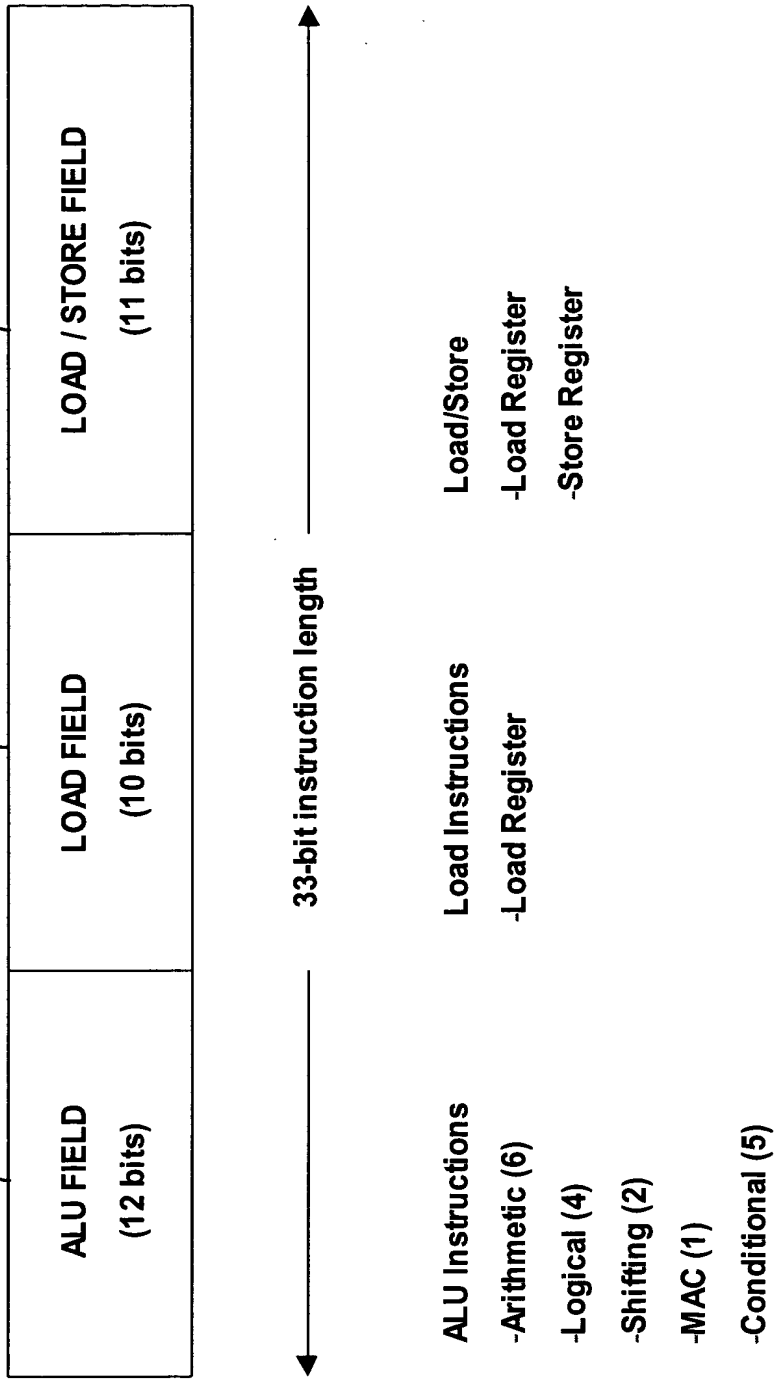
706
LOAD / STORE FIELD
(11 bits)
704
LOAD FIELD
(10 bits)
702
ALU FIELD
(12 bits)
33-bit instruction length
Load/Store
-Load Register
-Store Register
Load Instructions
-Load Register
ALU Instructions
-Arithmetic (6)
-Logical (4)
-Shifting (2)
-MAC (1)
-Conditional (5)

FIG. 7

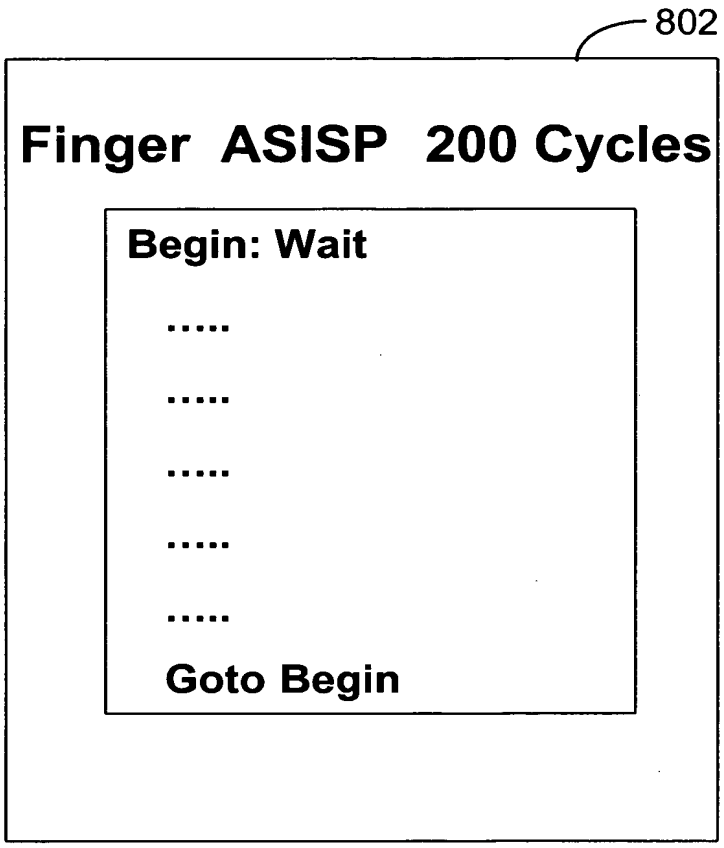

FIG. 8

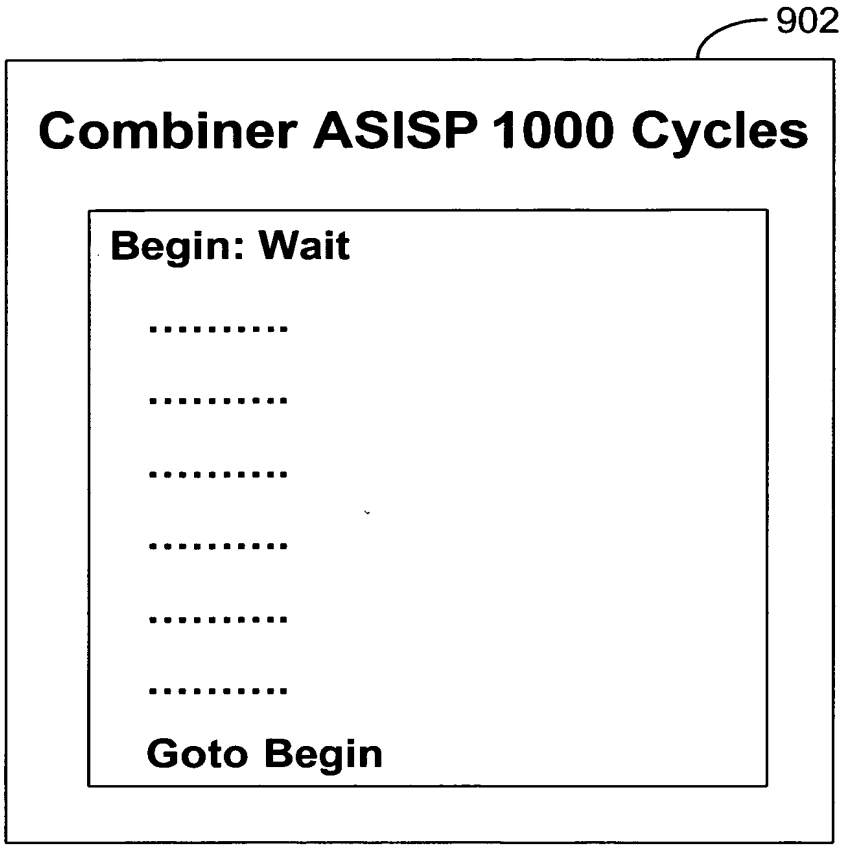

FIG. 9